**Creating a Dual Ported 8 register general REGISTER SET**

The register set is comprised of register lines. Each register line has the following arrangement.



The Interface

ABUS,BBUS INOUT std\_logic\_vector (15 downto 0);

Aload,Bload,Adrive,Bdrive IN std\_logic

Arsel,Brsel IN std\_logic

The register lines are then used to construct a register set, adding the 3 to 8 priority encoded to use the 3 bit register address to activate to select line on the given register. The output of the priority encoders are connected to the Arsel and Brsel inputs of the register lines.



Interface

ABUS,BBUS INOUT std\_logic\_vector (15 downto 0);

Aload,Bload,Adrive,Bdrive IN std\_logic

Aregno,Bregno IN std\_logic\_vector (2 downto 0)

**Assignment MTreg (200 pts)**

The assignment is to take the basic components of 3-to-8 priority encoder, busdriver, register and 2-to-1 mux and build up this 8 register structure. It will be structural plus a couple of concurrent signal assignment statements for the little bit of control logic.

Provided VHDL files are: reg16, mux2\_to\_1x16 ,busdr, and pri3to8 (each is .vhdl)

Testbenches are also provided.